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3 What is claimed is:

4 1. A method of fabrication of a capacitor comprising the steps of :

5 a) providing a semiconductor structure having a first region and a capacitor
6 region;

7 b) forming a first conductive layer over said semiconductor structure;

8 c) patterning said first conductive layer to form a plurality of trenches in said
9 capacitor region;

10 d) forming a capacitor dielectric layer over said first conductive layer;

11 e) forming a top plate over said capacitor dielectric layer in the capacitor region;

12 f) patterning said first conductive layer in said first region to form first
13 conductive patterns and a bottom plate;

14 g) forming an interlevel dielectric layer over said first conductive layer.

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16 2. The method of claim 1 which further includes forming interconnects to
17 electrically contact said top plate, said bottom plate and said first conductive patterns.

18 3. The method of claim 1 which further includes:

19 said first conductive pattern comprise a n-1 level wiring layer;

20 forming via contacts in said interlevel dielectric layer to contact said
21 top plate, said bottom plate and said first conductive patterns;

22 forming a second conductive line contacting said via contacts.

- 1 4. The method of claim 1 which further includes:
2 forming via contacts in said interlevel dielectric layer to contact said
3 top plate, said bottom plate and said first conductive patterns;
4 forming second conductive layer contacting said via contacts; said
5 second conductive layer is a n level metal layer; said first conductive patterns comprise a
6 n-l level metal layer.
- 7 5. The method of claim 1 wherein said first conductive layer is comprised of Al, Ti,
8 Ta, Cu and alloys of Al, Ti, Ta, or Cu; and has a thickness in the range of between
9 3000 and 10,000 Å.
- 10 6. The method of claim 1 wherein said plurality of trenches formed in a pattern of
11 rows and columns.
- 12 7. The method of claim 1 wherein said trenches extend down into the conductive layer
13 between 24 % and 84 % of the thickness of said first conductive layer.
- 14 8. The method of claim 1 wherein step (c) further comprises:
15 forming a trench resist layer over said first conductive layer; said
16 trench resist layer has openings that define areas where trenches will be formed in first
17 conductive layer in said capacitor area;
18 patterning said first conductive layer to form a plurality of trenches in
19 said capacitor region;
20 removing said trench resist layer.

- 1 9. The method of claim 1 wherein said capacitor dielectric layer has a thickness
2 between 100 and 1000 Å and is comprised of a material selected from the group
3 consisting of silicon oxide, silicon nitride, silicon oxide-nitride, and tantalum oxide.
- 4 10. The method of claim 1 wherein said top plate is formed by forming a top plate
5 layer over said capacitor dielectric layer; and masking and patterning said top plate
6 layer.
- 7 11. The method of claim 1 wherein step (f) further comprises: forming a bottom metal
8 resist mask over the first conductive layer; the bottom metal resist mask has openings
9 that define the interconnect lines;
10 patterning said first conductive layer in said first region to form first
11 conductive patterns and a bottom plate;
12 removing said bottom metal resist mask.
- 13
- 14 12. The method of claim 1 wherein said interlevel dielectric layer is comprised of oxide
15 formed using a high density plasma enhanced chemical vapor silicon oxide deposition
16 combined with plasma enhanced tetraethyl orthosilicate; and interlevel dielectric layer
17 is preferably planarized using a chemical-mechanical polish process.

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2 13. A method of fabrication of a capacitor comprising the steps of :

3 a) providing a semiconductor structure having a first region and a capacitor
4 region;

5 b) forming a first conductive layer over said semiconductor structure;

6 c) forming a trench resist layer over said first conductive layer; said trench
7 resist layer has openings that define areas where trenches will be formed in
8 first conductive layer in said capacitor area; then

9 d) patterning said first conductive layer to form a plurality of trenches in said
10 capacitor region; then

11 (1) said trenches extend down into the conductive layer between 24 %
12 and 84 % of the thickness of said first conductive layer;

13 e) removing said trench resist layer; then

14 f) forming a capacitor dielectric layer over said first conductive layer; then

15 g) forming a top plate over said capacitor dielectric layer in the capacitor region;
16 said top plate is formed by forming a top plate layer over said capacitor
17 dielectric layer; and masking and patterning said top plate layer; then

18 h) patterning said first conductive layer in said first region to form first
19 conductive patterns and a bottom plate; said first conductive patterns comprise
20 a n-l level metal layer;

- 1 i) forming an interlevel dielectric layer over said first conductive layer and said
2 top plate;
3 j) forming via contacts in said interlevel dielectric layer to contact said top
4 plate, said bottom plate and said first conductive patterns;
5 k) forming second conductive layer contacting said via contacts; said second
6 conductive layer is a n level metal layer.

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8 14. The method of claim 13 wherein said first conductive layer is comprised of Al, Ti,
9 Ta, Cu and alloys of Al, Ti, Ta, or Cu; and has a thickness in the range of between
10 3000 and 10,000 Å.

11 15. The method of claim 13 wherein said plurality of trenches formed in a pattern of
12 rows and columns.

13 16. The method of claim 13 wherein said top plate is formed by forming a top plate
14 layer over said capacitor dielectric layer; and masking and patterning said top plate
15 layer.

16 17. The method of claim 13 wherein step (h) further comprises: forming a bottom
17 metal resist mask over the first conductive layer; the bottom metal resist mask has
18 openings that define the interconnect lines;
19 patterning said first conductive layer in said first region to form first
20 conductive patterns and a bottom plate;
21 removing said bottom metal resist mask.